Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Withdrawn): A semiconductor device evaluation method comprising the steps of:

(a) for a plurality of insulated gate transistors with different channel lengths, determining an effective channel length Leff, a gate capacitance Cg which is a capacitance between a gate and a substrate, and a fringing capacitance Cf which is a capacitance between said gate and a portion of said substrate not covered with said gate, by electrical measurement and/or calculation;

(b) plotting said gate capacitance Cg and said effective channel length Leff, which have been determined in said step (a), on a graph and extending the same by extrapolation on said graph to determine gate-capacitance-vs.-effective-channel-length characteristics; and

(c) calculating a gradient A of said gate-capacitance-vs.-effective-channel-length characteristics and determining a finished gate length Lg for each of said plurality of insulated gate transistors from the equation, $Lg = (Cg - Cf)/A$.

Claim 2 (Withdrawn): The semiconductor device evaluation method according to claim 1, wherein

said step (a) prepares a design gate length Ld instead of determining said effective channel length Leff by electrical measurement and/or calculation,

said step (b) plots said gate capacitance Cg and said design gate length Ld, which have been determined in said step (a), on a graph and extends the same by extrapolation on

said graph to determine gate-capacitance-vs.-design-gate-length instead of determining said

gate-capacitance-vs.-effective-channel-length characteristics, and

said step (c) calculates a gradient of said gate-capacitance-vs.-design-gate-length

characteristics as said gradient A, instead of calculating the gradient of said gate-capacitance-

vs.-effective-channel-length characteristics.

Claim 3 (Withdrawn): The semiconductor device evaluation method according to

claim 1, wherein said step (b) carries out said extrapolation of said characteristics by linear

approximation.

Claim 4 (Withdrawn): The semiconductor device evaluation method according to

claim 1, further comprising the steps of:

(d) determining an intercept B of said gate-capacitance-vs.-effective-channel-length

characteristics; and

(e) for said plurality of insulated gate transistors, determining a gate overlap

capacitance CGDO which is a capacitance between said gate and a source/drain region

covered with said gate, from the equation, $CGDO = B/(2 \cdot W) - Cf$, by using a gate width W

of said gate.

Claim 5 (Withdrawn): The semiconductor device evaluation method according to

claim 1, further comprising the step of:

(f) for said plurality of insulated gate transistors, determining an effective gate

insulating film thickness Toxeff from the equation, $Toxeff = W - \epsilon ox / A$, by using said

gradient A, a gate width W of said gate, and the permittivity ϵox of a gate insulating film.

Claim 6 (Withdrawn): A computer-readable recording medium for recording a program which is executed by a computer either by itself or in combination with a preinstalled program in said computer, to carry out said semiconductor device evaluation method according to claim 1.

Claim 7 (Currently Amended): A semiconductor device evaluation apparatus comprising:

a calculation section ~~for~~configured to plot, for a plurality of insulated gate transistors with different channel lengths, ~~plotting~~ an effective channel length Leff and a gate capacitance Cg, which is a capacitance between a gate and a substrate, on a graph and ~~extending~~ to extend the same by extrapolation on said graph to determine gate-capacitance-vs.-effective-channel-length characteristics, and ~~calculating~~ to calculate a gradient A of said characteristics;

a first determination section ~~for determining~~configured to determine a finished gate length Lg for each of said plurality of insulated gate transistors from the equation, Lg = (Cg - Cf)/A, by using a fringing capacitance Cf which is a capacitance between said gate and a portion of said substrate not covered with said gate, said gradient A, and said gate capacitance Cg; and

a control section ~~for controlling~~configured to control said calculation section and said first determination section.

Claim 8 ( ): A semiconductor device evaluation apparatus comprising:

a calculation section configured to plot, for a plurality of insulated gate transistors with different channel lengths, a design gate length Ld and a gate capacitance Cg, which is a capacitance between a gate and a substrate, on a graph and to extend the same by

extrapolation on said graph to determine gate-capacitance-vs.-design-gate-length

characteristics, and to calculate a gradient A of said characteristics;

a first determination section configured to determine a finished gate length Lg for

each of said plurality of insulated gate transistors from the equation, Lg = (Cg - Cf)/A, by

using a fringing capacitance Cf which is a capacitance between said gate and a portion of said

substrate not covered with said gate, said gradient A, and said gate capacitance Cg; and

a control section configured to control said calculation section and said first

determination section

~~The semiconductor device evaluation apparatus according to claim 7, wherein~~

~~said calculation section uses a design-gate-length Ld instead of said effective channel~~

~~length Leff,~~

~~said calculation section plots said gate capacitance Cg and said design-gate length Ld~~

~~on a graph and extends the same by extrapolation on said graph to determine gate-~~

~~capacitance-vs.-design-gate-length characteristics, instead of determining said gate-~~

~~capacitance-vs.-effective-channel-length characteristics, and~~

~~said calculation section calculates a gradient of said-gate-capacitance-vs.-design-gate-~~

~~length-characteristics as said-gradient A, instead of calculating the gradient of said-gate-~~

~~capacitance-vs.-effective-channel-length characteristics.~~

Claim 9 (Currently Amended): The semiconductor device evaluation apparatus

according to claim 7, wherein

said calculation section ~~carries~~ is configured to carry out said extrapolation of said

characteristics by linear approximation.

Claim 10 (Currently Amended): The semiconductor device evaluation apparatus according to claim 7, wherein

said calculation section further ~~determines~~ configured to determine an intercept B of said gate-capacitance-vs.-effective-channel-length characteristics,

said apparatus further comprising:

a second determination section ~~for, for said plurality of insulated gate transistors, determining~~ configured to determine, for said plurality of insulated gate transistors, a gate overlap capacitance CGDO which is a capacitance between said gate and a source/drain region covered with said gate, from the equation, $CGDO = B /(2 \cdot W) - Cf$, by using a gate width W of said gate,

wherein said second determination section is also controlled by said control section.

Claim 11 (Currently Amended): The semiconductor device evaluation apparatus according to claim 7, further comprising:

a third determination section ~~for, for said plurality of insulated gate transistors, determining~~ configured to determine an effective gate insulating film thickness Toxeff for said plurality of insulated gate transistors from the equation, $Toxeff = W \epsilon ox /A$, by using said gradient A, a gate width W of said gate, and the permittivity ϵox of a gate insulating film,

wherein said third determination section is also controlled by said control section.

Claim 12 (Withdrawn): A semiconductor device evaluation method comprising the steps of:

(a) while regarding a plurality of insulated gate transistors with different gate length as a plurality of resistive elements with different line widths Lg each using a gate as a resistance, determining said line width Lg for some of said plurality of resistive elements;

(b) for all of said plurality of resistive elements, determining a resistance Rg of said gate and an effective channel length Leff by electrical measurement and/or calculation;

(c) plotting said line width Lg and said effective channel length Leff, which have been determined in said steps (a) and (b), on a graph and extending the same by extrapolation on said graph to determine line-width-vs.-effective-channel-width characteristics; and

(d) for all of said plurality of resistive elements, determining characteristics between said line width Lg and said resistance Rg by using said line-width-vs.-effective-channel-length characteristics.

Claim 13 (Withdrawn): A semiconductor device evaluation method comprising the steps of:

(g) preparing a finished gate length Lg determined by said semiconductor device evaluation method according to claim 1;

(h) for each of said plurality of insulated gate transistors, determining a resistance Rg of a gate by electrical measurement and/or calculation; and

(i) determining characteristics between said finished gate length Lg and said resistance Rg.

Claim 14 (Withdrawn): A computer-readable recording medium for recording a program which is executed by a computer either by itself or in combination with a preinstalled program in said computer, to carry out said semiconductor device evaluation method according to claim 12.

Claim 15 (Withdrawn): A semiconductor device evaluation apparatus comprising:

a calculation section for, while regarding a plurality of insulated gate transistors with different channel lengths as a plurality of resistive elements with different line widths Lg each using a gate as a resistance, plotting an effective channel length Leff and said line width Lg for some of said plurality of resistive 'elements on a graph and extending the same by extrapolation on said graph to determine line-width-vs.-effective-channel-length characteristics;

a determination section for, for all of said plurality of resistive elements, determining characteristics between said line width Lg and a resistance Rg of said gate by using said line-width-vs.-effective-channel-length characteristics; and

a control section for controlling said calculation section and said determination section.

Claim 16 (Withdrawn): A semiconductor device evaluation apparatus comprising:

a determination section for determining characteristics between a finished gate length Lg obtained by said semiconductor device evaluation method according to claim 1, and a resistance Rg of a gate for each of said plurality of insulated gate transistors; and

a control section for controlling said determination section.

Claim 17 (Withdrawn): A semiconductor device manufacturing control method comprising:

a judgment step for judging whether said finished gate length Lg of each of said plurality of insulated gate transistors, obtained by said semiconductor device evaluation method according to claim 1, meets required standard,

wherein a result of judgment in said judgment step is utilized for reappraisal of manufacturing conditions of semiconductor devices.

Claim 18 (Withdrawn): A semiconductor device manufacturing method comprising

a judgment step for judging whether said finished gate length Lg of each of said

plurality of insulated gate transistors, obtained by said semiconductor device evaluation

method according to claim 1, meets required standards,

wherein a result of judgment in said judgment step is utilized for rejection of

nonconforming products.

Claim 19 (Withdrawn): A semiconductor device manufacturing control method

comprising:

a judgment step for judging whether said resistance Rg of each of said plurality of

insulated gate transistors, obtained by said semiconductor device evaluation method

according to claim 12, meets required standards,

wherein a result of judgment in said judgment step is utilized for reappraisal of

manufacturing conditions of semiconductor devices.

Claim 20 (Withdrawn): A semiconductor device manufacturing method comprising:

a judgment step for judging whether said resistance Rg of each of said plurality of

insulated gate transistors, obtained by said semiconductor device evaluation method

according to claim 12, meets required standards,

wherein a result of judgment in said judgment step is utilized for rejection of

nonconforming products.

Claim 21. (New) The semiconductor device evaluation apparatus according to claim

8, wherein

said calculation section is configured to carry out said extrapolation of said characteristics by linear approximation.

Claim 22. (New) The semiconductor device evaluation apparatus according to claim 8, further comprising:

a second determination section configured to determine, for said plurality of insulated gate transistors, an effective gate insulating film thickness Toxeff from the equation, $Toxeff = W - \epsilon ox / A$, by using said gradient A, a gate width W of said gate, and the permittivity ϵox of a gate insulating film,

wherein said second determination section is also controlled by said control section.